High aspect ratio MEMS and CMOS: Collaborators or competitors?

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Abstract: As commercialisation of MEMS continues, integrated MEMS devices are under development, whereby the MEMS and CMOS or BICMOS technologies are brought together on the same chip. This technique is an alternative to hybrid packaging, where the MEMS and CMOS components are manufactured separately and bonded to complete the device. The cost of processing integrated MEMS devices has been analysed, using the MEMSCOST spreadsheet, showing that the MEMS component is only a few percent of the overall cost of manufacturing, even when a High-Aspect-Ratio (HAR) process is employed and even less when test and packaging costs are taken into account.

Keywords: cost modelling; MEMS; manufacturing cost; high aspect ratio; MEMSCOST; accelerometer; cantilever.

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Biographical notes: Ron A. Lawes is a Director of MiniFAB, a micro-nano-bio company based in Australia. He is a Visiting Professor at Imperial College, London and at Birmingham University in the UK. He was the Founding Director of the Central Microstructure Facility (CMF) at the Rutherford Appleton Laboratory in 1977 and remained its Director until he retired in September 2003. He was also Director of Engineering for the Rutherford Appleton and Daresbury Laboratories from 2001–2003. He was elected a Fellow of the Royal Academy of Engineering in 1995, Fellow of the Institution of Electrical Engineers in 1981 and a Fellow of the Institute of Physics in 1987. He is a Chartered Engineer, Physicist and Scientist.

1 Introduction

MEMS components based on CMOS-like surface microengineering have the advantage of a mature, low cost manufacturing technology compatible with a CMOS production line. This enables the designer to integrate the MEMS component, for example a sensor or actuator, with signal processing electronics all on the same silicon chip and as part of a continuous manufacturing process.

MEMS components based on High-Aspect-Ratio (HAR) microengineering have the advantage of higher sensitivity to external forces and the potential to evolve novel

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designs based on true micro-mechanical principles. While demonstrable in the R&D laboratory, commercial exploitation of such devices is often difficult, partly due to the apparent incompatibility of the HAR MEMS manufacture and the associated CMOS electronics and partly due to the perception that HAR techniques are too expensive.

The extent to which future MEMS devices can be manufactured solely by surface microengineering and eventually integrated with CMOS on a single production line is unclear. Some observers conclude that it is better to allow each technology to develop along separate lines and to concentrate on the technical and financial implications of producing the hybrid product. Others, that low cost will always favour the CMOS-like approach, whatever the technical limitations.

It will be assumed that production engineers will continue to defy such logic and develop the necessary compatibility between CMOS and HAR technology. The issue to be investigated here is the relative cost between the CMOS and the MEMS component of a device, whether integrated by an embedded CMOS-MEMS or hybrid approach.

2 Costing methodology

The cost of CMOS is well known with many options covering feature sizes (typically 0.09 um to 0.8 um), processed layers per die (typically 14–36) and wafer diameters (typically 100–300 mm). The cost of MEMS is far less discussed, particularly as the process technology is often unique to each MEMS device. The relative costs between CMOS and MEMS are rarely available in the public domain.

Commercial simulation packages to estimate CMOS wafer and die costs have been available for many years and have been continually improved in scope and accuracy (IC Knowledge, 2007). Recently, the commercial packages have been extended to include the cost of a number of MEMs foundry processes, particularly those using silicon surface microengineering. There is little information in the public domain as to the accuracy of such packages and the exact methods of data handling are naturally proprietary. Consequently, a cost simulation package MEMSCOST (Lawes, 2007) has been developed specifically to enable the relative cost of MEMS and CMOS-like processes to be studied, either separately or together, as a single production line.

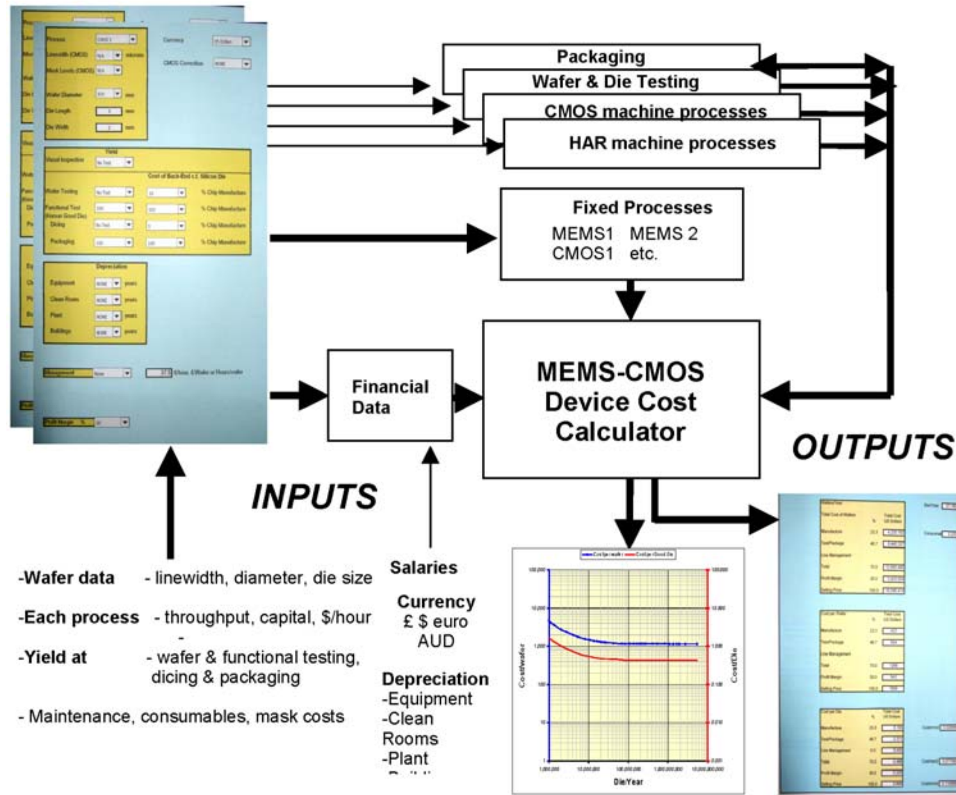
MEMSCOST has modelling algorithms for the major HAR processes i.e., DRIE, Excimer Laser Ablation, LIGA (UV and X-ray), bulk silicon micromachining and various forms of Wafer Bonding (anodic, eutectic, frit etc.). MEMSCOST also has modelling algorithms for the major CMOS-like processes e.g., aligner and stepper lithography, dc and rf sputter deposition, CVD, furnace oxidation, dry plasma and wet etching, implantation etc. A surface microengineering lithography process is included. For each machine in the process, standard or custom parameters can be input for capital and maintenance costs, throughput/hour or time/process step.

Complete processes may be set from a list containing standard steps and the number of layers/wafer defined for that particular process step. Financial data includes hours/shift, salary levels, overhead rate and depreciation of equipment, clean rooms, plant and buildings. Currency conversion is readily available.

Wafer testing, functional die testing can be modelled along with dicing wire/flip-chip bonding and packaging. Yields can be specified at each step.

Calculations are done on a fixed plus variable costs basis or cost/hour for each process listed. Outputs include the total cost in the selected currency for basic chip manufacture, testing and packaging. A profit margin can be set, a selling price calculated and hence turnover estimated. Results can be set for the cost/wafer and the cost/die (tested or untested). A schematic diagram illustrating the structure of MEMSCOST is shown in Figure 1.

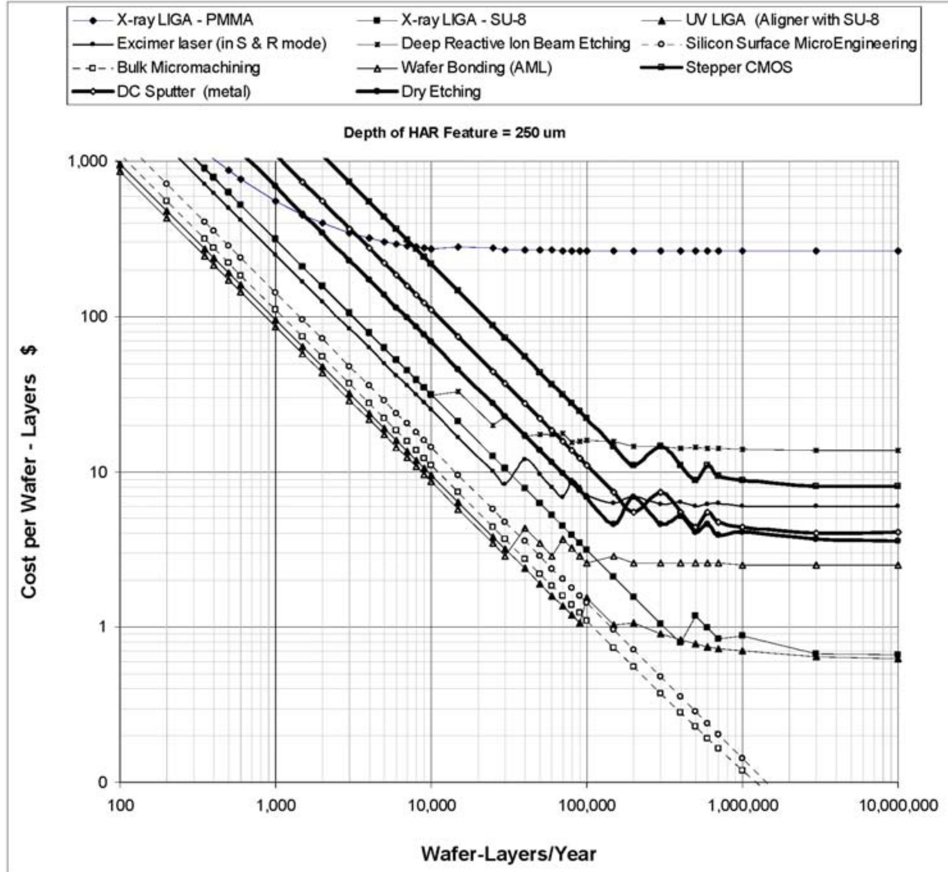
Figure 1 Schematic of the MEMS costs spreadsheet MEMSCOST (see online version for colours)



A typical output for some individual processes is shown in Figure 2. Here a comparison can be made between different HAR MEMS processes and some of the CMOS-like processes e.g., thin film metal deposition and plasma etching. Note the high expense of optical stepper technology.

Despite the higher cost of HAR MEMS techniques, a device so constructed will have far fewer processed layers e.g., <100 than with current CMOS (e.g., 200–300), many of which will be non-HAR such as thin film metal deposition. Therefore, when making cost comparisons between an HAR-based and a CMOS-based MEMS device, the total manufacturing processes should be taken into account.

Figure 2 Cost/wafer for some MEMS HAR and CMOS processes as a function of wafer output



3 Some CMOS-MEMS examples

Currently available accelerometers are convenient to analyse as they are examples of an integrated CMOS-MEMS device, that are high performance, rely upon an HAR process (DRIE) and use an established (Bi-CMOS) process to manufacture the signal processing electronics.

There is considerable debate as to the cost of testing and packaging. It is often reported that assembly, packaging and testing take up 70–80% of the manufacturing costs for a MEMS device. A similar figure (66%) is available from industry (Sulouff, 2004) and will be used in the following calculations.

Table 1 shows a breakdown of the cost of a CMOS-MEMS integrated accelerometer of fictional design consisting of a 2.5×2.5 mm die on 200 mm wafers with a 50 um deep proof mass manufactured by DRIE and 0.25 um 28 layer CMOS technology. The yield is assumed to be 100%.

Table 1 Cost structure for a CMOS-MEMS accelerometer

	DRIE		*X-ray LIGA with SU-8 resist*	
Process	$	%	$	%
HAR- processes	41	2.2	75	4.0
CMOS-like processes	1789	97.8	1789	96.0
Cost of wafer	1830	100	1864	100
Cost/Die (4757/wafer)	0.385		0.392	
Test	0.385		0.392	
Package	0.385		0.392	
Cost of manufacture	1.155		1.176	
Selling price	2.310		2.352	+1.8
10,000 wafers/year				47 million devices

The HAR DRIE step represents only approximately 2% of the manufacturing cost of the wafer and about 0.4% of the selling price. Even replacing the DRIE step with an X-ray LIGA step, a technology deemed by many to be too expensive (whatever the practical impediments), may be acceptable from a cost point of view should the performance benefits be desirable.

Interestingly, even the cost of a MEMS device perceived as manufactured from non-CMOS processes is not necessarily dominated by the HAR steps. Table 2 shows a breakdown of the cost of a MEMS device based on cantilever structures and excluding any CMOS microelectronics. The wafer size is 2.5×2.5 mm on 200 mm wafers and the yield is assumed to be 100%.

Even though the design does not contain the signal processing electronics, a significant fraction of the cost of manufacture goes into thin film CMOS-like processes. However, adding a further MEMs process in such a device starts to have a significant affect on overall cost.

Table 2 Cost structure for a MEMS cantilever device

	Wafer- Bond		*Wafer –Bond + DRIE*	
Process	$	%	$	%
HAR- processes	20	2.5	62	7.4
CMOS-like processes	777	92.2	777	92.6
Cost of wafer	797	100	839	100
Cost/Die (4757/wafer)	0.168		0.176	
Test	0.168		0.176	
Package	0.168		0.176	
Cost of manufacture	0.504		0.528	
Selling price	1.00		1.056	+5.6
10,000 wafers/year				47 million devices

4 Some comments

- The additional cost of a MEMS High Aspect Ratio process step, desirable for performance reasons, may add only a few percent to the manufacturing cost of an integrated CMOS-MEMS device and even less to its selling price.
- MEMS devices use a significant number of CMOS-like process steps so that even a typical MEMS device, based on cantilevers, might have less than10% of its manufacturing cost attributed to an HAR process. Even less to its selling price.
- Adding multiple HAR process steps will rapidly increase the cost of a device.
- The cost structure of only two MEMS examples have been studied in some detail. In practice the market will decide whether the performance – cost benefits of using one or more HAR processes are justified.
- It follows that cost alone may not be the impediment to the growth of HAR processes in integrated CMOS-MEMS devices but rather the technical difficulties of integrating two fundamentally different process on to a single product line.

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